Client's ref.:TSMC2002-0009/03-01-20 File:0503-7969USf/Robert/Steve

What Is Claimed Is:

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- A receiver circuit for outputting signals to an 1 internal circuit supplied with a first power supply voltage, 2 comprising: 3 a reference voltage circuit supplied with the first power 4 supply voltage for outputting a reference voltage 5 that is a mid-point voltage between the first power 6 supply voltage and ground; 7 a reference current circuit for generating a first current 8 9 according to the reference voltage; and a receiving circuit supplied with a second power supply 10 voltage higher than the first power supply voltage, 11 comprising: 12 a first current source for generating a second 13 current according to the first current; and 14 a differential amplifier circuit for generating an 15 output signal contained within a voltage range 16 of the first power supply voltage and centered 17 around the mid-point voltage to the internal 18
 - 2. The receiver circuit as claimed in claim 1, wherein
 the internal circuit comprises a plurality of transistors having
 a first gate oxide thickness.

circuit according to the second current.

3. The receiver circuit as claimed in claim 2, wherein the reference voltage circuit comprises a first PMOS transistor and a first NMOS transistor having the first gate oxide thickness.

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- 1 4. The receiver circuit as claimed in claim 3, wherein 2 the first PMOS transistor and the first NMOS transistor have a 3 first p/n ratio.
- 5. The receiver circuit as claimed in claim 4, wherein the transistors of the internal circuit have the first p/n ratio.
 - 6. The receiver circuit as claimed in claim 3, wherein the first PMOS transistor and the first NMOS transistor are connected in serial and between the first power supply voltage and ground, and the gates and the drains of the first PMOS transistor and the first NMOS transistor are connected.
- 7. The receiver circuit as claimed in claim 4, wherein the reference current circuit comprises:
 - a comparator circuit having a reverse input terminal, a non-reverse input terminal coupled to the gates of the first PMOS transistor and the first NMOS transistor, and an output terminal;
 - a first resistor coupled between the reverse input terminal and ground; and
 - a second current source coupled between the second power supply voltage and the first resistor for generating the first current flowing through the first resistor and generating the mid-point voltage at the connection point of the first resistor and the reverse input terminal.
 - 8. The receiver circuit as claimed in claim 1, wherein the second current is referenced to the first current by a current mirror or equivalent circuitry.

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the differential amplifier circuit comprises:

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2	a second DMOC transistor having a first source sounled to
3	a second PMOS transistor having a first source coupled to
4	the second current source, a first gate coupled to
5	an I/O signal, and a first drain;
6	a third PMOS transistor having a second source coupled to
7	the second current source, a second gate coupled to
8	a reverse I/O signal, and a second drain;
9	a second resistor coupled between the connection point of
LO	the first drain and the internal circuit, and ground;
L1	and
L2	a third resistor coupled between the connection point of
L3	the second drain and the internal circuit, and
L4	ground.
1	10. The receiver circuit as claimed in claim 7, wherein
2	the second and third PMOS transistors have a second gate oxide
3	thickness larger than the first gate oxide thickness.
1	11. The receiver circuit as claimed in claim 9, wherein
2	the resistances of the second and third resistor are the same.
1	12. The receiver circuit as claimed in claim 1, wherein
2	the mid-point voltage is approximately a switching point voltage
3	of the internal circuit.
1	13. A receiver circuit, comprising:
2	an internal circuit supplied with a first power supply
3	voltage and comprising a plurality of transistors
4	having a first p/n ratio and a first gate oxide
_	-
5	thickness;

The receiver circuit as claimed in claim 7, wherein

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- a reference voltage circuit supplied with the first power 6 supply voltage and comprising a first PMOS transistor 7 and a first NMOS transistor having a first p/n ratio 8 9 and the first gate oxide thickness, for outputting a reference voltage that is a mid-point voltage 10 between the first power supply voltage and ground; 11 a reference current circuit for generating a first current 12 according to the reference voltage; and 13 a receiving circuit supplied with a second power supply 14 voltage higher than the first power supply voltage, 15 comprising: 16 a first current source for generating a second 17 current according to the first current; and 18 a differential amplifier circuit for generating an 19 output signal contained within a voltage range 20 of the first power supply voltage and centered 21 around the mid-point voltage to the internal 22 circuit according to the second current. 23
 - 14. The receiver circuit as claimed in claim 13, wherein the first PMOS transistor and the first NMOS transistor are connected in serial and between the first power supply voltage and ground, and the gates and the drains of the first PMOS transistor and the first NMOS transistor are connected.
 - 15. The receiver circuit as claimed in claim 13, wherein the reference current circuit comprises:
 - a comparator circuit having a reverse input terminal, a non-reverse input terminal coupled to the gates of

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5	the first PMOS transistor and the first NMOS
6	transistor, and an output terminal;
7	a first resistor coupled between the reverse input terminal
8	and ground; and
9	a second current source coupled between the second power
10	supply voltage and the first resistor for generating
11	the first current flowing through the first resistor
12	and generating the mid-point voltage at the
13	connection point of the first resistor and the
14	reverse input terminal.
1	16. The receiver circuit as claimed in claim 13, wherein
2	the second current is referenced to the first current by a
3	current mirror or equivalent circuitry.
3	current mirror or equivarent circuitry.
1	17. The receiver circuit as claimed in claim 15, wherein
2	the differential amplifier circuit comprises:
3	a second PMOS transistor having a first source coupled to
4	the second current source, a first gate coupled to
5	an I/O signal, and a first drain;
6	a third PMOS transistor having a second source coupled to
7	the second current source, a second gate coupled to
8	a reverse I/O signal, and a second drain;
9	a second resistor coupled between the connection point of
10	the first drain and the internal circuit, and ground;
11	and
12	a third resistor coupled between the connection point of
13	the second drain and the internal circuit, and
14	ground.

Client's ref.: VIT03-0053/03-01-20 File:0608-7969USf/Robert/Kevin

- 1 18. The receiver circuit as claimed in claim 17, wherein 2 the second and third PMOS transistors have a second gate oxide 3 thickness larger than the first gate oxide thickness.
- 1 19. The receiver circuit as claimed in claim 17, wherein the resistances of the second and third resistor are the same.
- 1 20. The receiver circuit as claimed in claim 13, wherein 2 the mid-point voltage is approximately a switching point voltage 3 of the internal circuit.